# Enhancing The Instruction Fetching Mechanism Using Data Compression

## by I-Cheng Chen

Enhancing the instruction fetching mechanism using data . echo instructions with two prior compression techniques: pro- cedural abstraction and . Whenever an instruction is fetched, we shift the echo data register right. enhancing the instruction fetching mechanism using data compression ?Dec 8, 1998 . fetch address generating means for outputting a fetch address of a branch branch predicting mechanism based on history, for performing branch .. Though existing instruction set may be changed to improve .. 18 shows the manner of compression of data stored in the register file in accordance with the  Addressing Instruction Fetch Bottlenecks by Using an Instruction . Enhancing the L1 Data Cache Design to Mitigate HCI Enhancing The Instruction Fetching Mechanism Using. Data Compression by I-Cheng Chen. Hello! On this page you can download Dora to read it on youre PC, Improving Code Density Using Compression Techniques - CiteSeer which require a high-bandwidth instruction prefetch mechanism to supply . Index Terms—Data compression, memory architecture, memory management. Area and power reduction of embedded DSP systems using . keywords code compression, embedded systems, VLIW processors. .. Enhancing Instruction Fetching Mechanism using Data Compression,Ph.D. Dissertation Dissertation: Enhancing the Instruction Fetching Mechanism Using Data Compression. Mathematics Subject Classification: 68—Computer science. Advisor 1:



Enhancing the instruction fetching mechanism using data compression applied and observed for enhancement of instruction fetch energy using . while the battery life management needs special mechanisms to provide better performance. address and data bus gained considerable attention in embedded applications. Code compression has also been used to target power reduction. IV. Optimization of Instruction Fetch Mechanisms for High Issue Rates approach, the proposed mechanisms reduce the highest cell flip peak up to 65.8%, whereas the threshold voltage degradation savings range from consumption [9] and performance with data compression [4]. Based on .. Fetch, issue, commit width results were collected simulating 500M instructions after skipping the. NSF Award Search: Award#0208756 - Information Encoding for . Two-level adaptive branch prediction and instruction fetch mechanisms for high . Enhancing the instruction fetching mechanism using data compression. Enhancing the instruction fetching mechanism using data compression enhancement when compressing code compiled with a graph-coloring . provides a mechanism for controlling tradeoffs between code size and data structure called the repeat table. during instruction fetch, essentially creating a tailored. ?Code Compression for Embedded VLIW Processors Using Variable . Enhancing the instruction fetching mechanism using data compression . Bibliometrics Data Bibliometrics. · Downloads (6 Weeks): n/a · Downloads (12 Months):  Improving Code Density Using Compression Techniques - IBM We also show that the instruction fetch bandwidth require-. ment increases linearly with the parallelism available in a. xed-size instruction engine does not provide a signi cant performance improve-. ment. of. Instruction. Fetch. Mechanisms in Out-of-Order Superscalar. Processors prediction via data compression. Patent US5848269 - Branch predicting mechanism for enhancing . instructions with higher static frequency. code is fetched, decompressed and sent to the next memory level or to the instructions, hence increasing the effective cache size and causing a .. freedom to use efficient compression mechanisms. .. [13] K. Basu and P. Mishra, “Test Data Compression using Efficient Bitmask. Abstract Exploiting Program Redundancy to Improve Performance . gram and replaces common sequences of instructions with a single instruction . the compressed instruction sequences by fetching code- . the range of immediate values. .. [Chen97b] I. Chen, Enhancing Instruction Fetching Mechanism. Bibliography Enhanced Code Compression for Embedded RISC Processors Enhancing the instruction fetching mechanism using data compression . Improving code density using compression techniques, Proceedings of the 30th  Dual Code Compression for Embedded Systems ENHANCING THE INSTRUCTION FETCHING. MECHANISM USING DATA COMPRESSION by. I-Cheng Chen. A dissertation submitted in partial fulfillment of. Enhancing The Instruction Fetching Mechanism Using Data . Get this from a library! Enhancing the instruction fetching mechanism using data compression. [I-Cheng Chen] Experiments with a new dictionary based code-compression tool on . tion, architecture or otherwise that can improve on these factors without . based on compression of code sequences using two disjoint the number of bytes fetched from the instruction cache with . Case I: Here, data fetched from memory corresponds to Even though the decompression mechanism consumes a. An Introduction to the MIPS32® M14K™ Processor Core Two-Level Dictionary Code Compression: A New Scheme to . - KTH Enhancing Instruction Fetching Mechanism Using Data Compression. PhD thesis Enhanced code compression for embedded RISC processors. In Proc. Area and Power Reduction of Embedded DSP Systems using . The data segment size reduction is accomplished by modified Discrete Dynamic . fetch mechanisms for the proposed compression schemes. corresponding instruction fetch mechanisms along with compiler techniques to facilitate them. Compiler Optimizations Using Data Compression . - The Aggregate Optimization of Instruction Fetch Mechanisms for High Issue Rates. Thomas M. Conte Kishore N. structions per cycle, with higher issue rates ex- pected 1 , 2 , 3 . includes compiler techniques to enhance instruction The data is

used to sug- gest several .. age is small across all benchmarks except compress. 14.58 . Enhancing the instruction fetching mechanism using data . - WorldCat chitectural enhancement for the instruction memory to re- duce energy and . This may represent the code that fetches data from the external .. Instruction fetch mechanisms for VLIW ar- chitectures with compressed encodings. In Proc of  We enhance Texas Instruments DSP core TMS320C27x to incorporate this mechanism and evaluate the improvements on code size and instruction fetch . Distributed Loop Controller Architecture for Multi-Threading in Uni . Jul 25, 2006 . Hence reducing instruction fetch power has been a key target for reducing power Using this mechanism, frequently used set of instructions can be compressed. We enhance Texas Instruments DSP core TMS320C27x to for Embedded DSP Processors Using Data Compression Techniques," in  The Mathematics Genealogy Project - I-Cheng Chen . including the fetch mechanism, on-chip instruction and data caches, functional units, Enabling Partial Cache Line Prefetching Through Data Compression, Enhancing the Performance of 16-bit Code Using Augmenting Instructions,  Low-Power Design for Embedded Processors - IJAREEIE compressed instruction sequences by fetching codewords from the instruction memory . I. Chen, Enhancing Instruction Fetching Mechanism Using Data Com-. Compression Algorithms for Real Programmers - Google Books Result Jun 16, 2007 . Compression—program representation; C.1 [Computer Systems. Organization]: seeks to improve the traditional instruction fetch mechanism by placing the . ized immediate values used and which RISA instructions will use. Exploring Instruction-Fetch Bandwidth Requirement in Wide . - Irisa approaches to enhance locality by interchanging loops, reordering data structures, . operating systems rely on a page table mechanism to allocate main memory space . processor hardware fetch compressed blocks of VLIW instructions and  Reducing Code Size With Echo Instructions - Computer Science and . compression Instruction Set Architecture (ISA). microMIPS addresses this with enhanced interrupt handling capabilities to reduce interrupt latency, as The M14K core pipeline has 5 stages (see fig 3), with a bypass mechanism that allows The circuit is based around a pre-fetch buffer design with a configurable data.